CLAIMS

What is claimed is:

1. A test logic for testing operation of an electronic circuit, comprising:

a source that provides a plurality of test signals to a plurality of input ports of the electronic circuit;

a plurality of tester IO channels that carry a first subset of a plurality of output signals from corresponding output ports of the electronic circuit; and

an observe logic module that processes a second subset of the plurality of output signals in order to provide at least one processed signal, the at least one processed signal being generated from the second subset of the plurality of output signals.

2. The test logic of claim 1, further comprising:

an interface module that enables the user to determine whether a section of the electronic circuit is properly operating by generating at least one observable signal, the at least one observable signal being derived from the at least one processed signal, the section of the electronic circuit being associated with the second subset.

3. The test logic of claim 1, wherein the observe logic module includes a signature compactor.

4. The test logic of claim 3, wherein the signature compacter comprises:

a set of linear feedback shift registers (LFSR), wherein an input signal to the set of linear feedback shift registers corresponds to a corresponding output port of the electronic circuit, and wherein a LFSR output signal corresponds to the at least one processed signal.

5. The test logic of claim 4, wherein the set of linear feedback shift registers corresponds to a multiple input shift register structure, and wherein the multiple input shift register structure receives a plurality of input signals, each input signal corresponding to an associated output port of the electronic circuit.

6. The test logic of claim 3, wherein the signature compacter comprises:

a set of linear cellular automata registers, wherein an input signal to the set of linear cellular automata registers corresponds to a corresponding output port of the electronic circuit, and wherein an output of the linear cellular automata registers corresponds to the at least one processed signal.

7. The test logic of claim 1, wherein the source comprises a pattern generator that generates a first set of test signals, each of the first set of test signals being applied one of a plurality of input ports of the electronic circuit.

8. The test logic of claim 2, wherein the interface module includes a comparator that compares the at least one processed signal with a predetermined value to provide the at least one observable signal.

9. The test logic of claim 2, wherein the interface module includes a register that stores a result generated by the observe logic module.

10. The test logic of claim 2, further comprising:

a processor module that reads the at least one observable signal to determine whether the section of the electronic circuit is operating properly.

11. The test logic of claim 7, further comprising:

a multiplexer that selectively couples either the first set of test signals or a second set of test signals to a plurality of multiplexer output ports, the second set of test signals being generated by another source, each multiplexer output port being connected to a corresponding input port of the electronic circuit.

12. The test logic of claim 1, wherein the observe logic module comprises a comparator that compares the second subset of the plurality of output signals with a predetermined value to obtain the at least one processed signal.

13. The test logic of claim 1, wherein the electronic circuit comprises a component of the test logic.

14. A method for testing operation of an electronic circuit, comprising:

(a) providing a plurality of test signals to an electronic device;

(b) partitioning a plurality of output signals into a first subset and a second subset, each of the plurality of output signals being associated with an output port of the electronic device;

(c) coupling the first subset to a plurality of tester IO channels; and

(d) processing the second subset to obtain at least one processed signal, the at least one processed signal being generated from the second subset.

15. The method of claim 14, further comprising:

(e) generating at least one observable signal that is indicative whether a section of the electronic circuit is operating properly, the at least one observable signal being derived from the at least one processed signal.

16. The method of claim 14, wherein the electronic device comprises an integrated circuit.

17. The method of claim 15, further comprising:

(f) analyzing the at least one observable signal to determine whether the section of the electronic circuit is operating properly.

18. The method of claim 14, wherein (a) comprises:

(i) selecting either a first set of test signals or a second set of test signals to obtain the plurality of test signals, the first set being generated by a pattern generator and the second set being generated by another source; and

(ii) applying the selected test signals to the electronic device.

19. The method of claim 14, wherein (d) comprises:

(i) comparing the second subset with a predetermined value: and

(ii) in response to (i), setting a value of the at least one processed signal.

20. The method of claim 14, wherein (d) comprises:

(i) generating the at least one processed signal, wherein the at least one processed signal is generated from the second subset of the plurality of output signals.

21. The method of claim 15, wherein (e) comprises:

(i) comparing the at least one processed signal with a predetermined value; and

(ii) in response to (i), setting a value of the at least one observable signal.

22. The method of claim 18, wherein the pattern generator is supported by a component of a test logic.

23. The method of claim 15, wherein one of the at least one observable signal is observable through an IO channel.

24. The method of claim 15, wherein the at least one observable signal is identical or substantially identical to the at least one processed signal.

25. The method of claim 18, wherein the predetermined value is obtained from a processor module.

26. A test logic for testing operation of an electronic circuit, comprising:

a pattern generator that generates a set of test signals, each of the set of test signals corresponding to one of a plurality of input ports of the electronic circuit;

a plurality of tester IO channels that carry a first subset of a plurality of output signals from corresponding output ports of the electronic circuit;

a signature compactor that processes a second subset of the plurality of output signals in order to provide at least one processed signal, the at least one processed signal being generated by the second subset of the plurality of output signals, the signature compactor including a set of linear feedback shift registers, wherein an input signal to the set of linear feedback shift registers corresponds to a corresponding output port of the electronic circuit, and wherein an output signal of the set of linear feedback shift registers corresponds to a corresponding processed signal; and

an interface module that enables determination of whether a section of the electronic circuit is properly operating from at least one observable signal, the at least one observable signal being derived at least in part from the at least one processed signal, the section of the electronic circuit being associated with the second subset of the plurality of output signals.